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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/711,416	09/17/2004	Bruce B. Doris	FIS920040105	5415	
45094	45094 7590 09/29/2006			EXAMINER	
HOFFMAN, WARNICK & D'ALESSANDRO LLC			HARRISON, MONICA D		
75 STATE ST 14TH FL			ART UNIT	PAPER NUMBER	
ALBANY, NY 12207			2813		

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary Diriti,416			Application No.	Applicant(s)					
Monica D. Harrison 2813			10/711,416	DORIS ET AL.					
The MALING DATE of this communication appears on the cover sheet with the correspondence address—Period for Repty A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of turn may be a relation under the provisions of 2 FCR 1.136(). In a reveal, however, may sery be timely fined in the provisions of 2 FCR 1.136(). In a reveal, however, may sery be timely fined in the provision of the provision of the provision of 2 FCR 1.136(). In a reveal, however, may sery be timely fined in the provision of 2 FCR 1.736(). Bright for reply is prodicted above, the maximum distiloting yearled will seply and will seply and will sery to Story Months from the realiting date of this communication. Pellution to reply which he sect or elated period for reply is prodicted period for reply is prodicted period for reply is prodicted period for reply is produced by the College of the produced of the produ		Office Action Summary	Examiner	Art Unit					
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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10-17, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bryant et al (US 2005/0285187 A1).

- Regarding claim 1, Bryant et al discloses a semiconductor device structure comprising: at least two active regions having different surface directions (Figure 4, references 120 and 140), each active region including one of a plurality of nFETs (Figure 4, reference 20) and a plurality of pFETs (Figure 4, reference 45), and wherein a gate electrode orientation is such that the nFETs and the pFETs are substantially parallel to each other (Figure 4, reference 5).
- 2. Regarding claim 2, Bryant et al discloses wherein the pFETs are located in an active region with a current flow in a <11 0> surface direction, and the nFETs are located in an active region with a current flow in a <1 00> surface direction (Figure 4).
- Regarding claim 3, Bryant et al discloses wherein the pFETs are located in an active region with a (110) surface orientation and a <111 > surface direction, and the nFETs are located in an active region with a (100) surface orientation and a <110 > surface direction (Figure 4).

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4. Regarding claim 4, Bryant et al discloses further comprising means for applying: a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET (Figure 4, references 25 and 55); and a tensile stress in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET (pg.5, paragraph 0077).

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- 5. Regarding claim 5, Bryant et al discloses a method of forming a semiconductor device structure, the method comprising the steps of: bonding a first wafer having a first surface direction atop a second wafer having a different second surface direction (Figure 4, references 9, 15 and 17); forming an opening through the first wafer to the second wafer (Figure 4, reference 70); and forming a region in the opening coplanar with a surface of the first wafer, wherein the region has the second surface direction (Figure 4, reference 70).
- Regarding claim 10, Bryant et al discloses wherein each wafer includes a silicon layer on an insulator layer (Figure 4, references 9, 15 and 17), and the opening forming step includes forming the opening to the silicon layer of the second wafer (Figure 4, reference 70).
- 7. Regarding claim 11, Bryant et al discloses wherein the region forming step includes epitaxially growing silicon in the opening, and planarizing the silicon (pg.4, paragraph 0064).
- 8. Regarding claim 12, Bryant et al discloses wherein the opening forming step includes forming a sidewall spacer along the opening (Figure 4, reference 4).
- 9. Regarding claim 13, Bryant et al discloses wherein the first surface direction is a <100> surface direction and the second surface direction is a <110> surface direction (Figure 4).

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- 10. Regarding claim 14, Bryant et al discloses wherein the first surface direction is a <110> surface direction and the second surface direction is a <111 > surface direction (Figure 4).
- 11. Regarding claim 15, Bryant et al discloses wherein the first wafer has a first surface orientation and the second wafer has a different second orientation, and the region has the second surface orientation (Figure 4).
- 12. Regarding claim 16, Bryant et al discloses wherein the first surface direction and the second surface direction are selected to degrade mobility (Figure 4).
- 13. Regarding claim 17, Bryant et al discloses a method of forming a semiconductor device structure, the method comprising the steps of: bonding a first wafer having a first surface direction and a first surface orientation atop a second wafer having a different second surface direction and a different second surface orientation (Figure 4, reference 9, 15 and 17); forming an opening through the first wafer to a silicon layer of the second wafer (Figure 4, reference 70); generating a silicon in the opening to a surface of the first wafer, wherein the silicon has the different second surface orientation (Figure 4); forming a plurality of pFETs on the silicon (Figure 4, reference 45), and a plurality of nFETs on another region of the first wafer (Figure 4, reference 20), wherein gate electrodes of the FETs are substantially parallel to one another (Figure 4, reference 5); and applying at least one of a filled trench configuration and at least one process to provide (Figure 4, reference 70): a compressive stress in a longitudinal direction with respect to a current flow of the pFETs and a transverse direction with respect to a current flow of the nFETs (Figure 4, reference 55); and a tensile stress in a longitudinal direction with respect to a current flow of the nFETs and a transverse direction with respect to a current flow of the pFETs (pg.5, paragraph 0077).

14. Regarding claim 19, Bryant et al discloses wherein each wafer includes a silicon layer on an insulator layer (Figure 4), and the opening forming step includes forming the opening to the silicon layer of the second wafer (Figure 4, reference 70).

15. Regarding claim 20, Bryant et al discloses wherein the region generating step includes epitaxially growing silicon in the opening, and planarizing the silicon, and the opening forming step further includes forming a sidewall spacer along the opening (pg.4, paragraph 0064).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al (US 2005/0285187 A1) in view of Machesney et al (5,670,388).

Bryant et al discloses all above claimed subject matter except implanting oxygen and annealing to form a buried oxide layer (claims 6 and 18).

Machesney et al discloses implanting oxygen and annealing to form a buried oxide layer (column 8, lines 35-54).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bryant et al with the teachings of Machesney et al, for the purpose of forming a body substrate connector for an SOI FET.

17. Regarding claim 7, Bryant et al discloses further comprising the step of forming a first type gate electrode on the region, and a second type gate electrode on another region of the first wafer, and all of the gate electrodes are substantially parallel to one another (Figure 4, reference 5).

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- 18. Regarding claim 8, Bryant et al discloses wherein the first gate electrode includes a pFET (Figure 4, reference 45), and the second gate electrode includes an nFET (Figure 4, reference 20).
- 19. Regarding claim 9, Bryant et al discloses further comprising the step of applying at least one of a filled trench configuration and at least one film to provide: a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET (Figure 4, references 25 and 55); and a tensile stress applied in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET (pg.5, paragraph 0077).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Monica D. Harrison AU 2813

mdh

September 21, 2006

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